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FIG. 1

Applicant(s): Minoru Maeda
PHASE LOCKED LOOP CIRCUIT USING FRACTIONAL
FREQUENCY DIVIDER

FIG. 2

FIG. 3

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FIG. 4

Fi ⟶ [DDS $G/2^h$] ⟶ Fo

FIG. 5

1 — (~) ⟶ 2 [FPD] ⟶ 3 [FIL] ⟶ 4 (~) ⟶ Fout

5 — [FRACTIONAL FREQUENCY DIVISION $1/(M + A/B)$]

FIG. 6

REFERENCE SIGNAL (~)

SYNCHRONOUS INPUT ⟶ [HIGH-FREQUENCY SIGNAL GENERATOR-1]

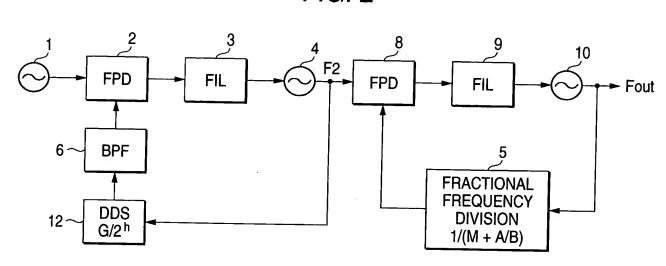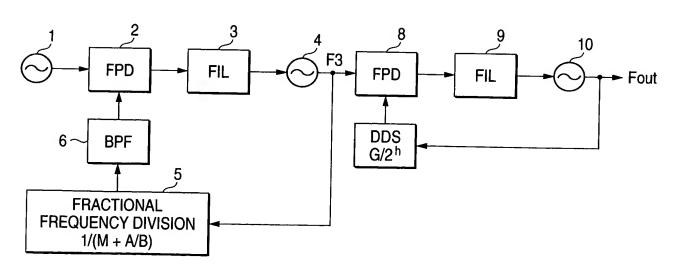SYNCHRONOUS INPUT ⟶ [HIGH-FREQUENCY SIGNAL GENERATOR-2]

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Applicant(s): Minoru Maeda
PHASE LOCKED LOOP CIRCUIT USING FRACTIONAL
FREQUENCY DIVIDER

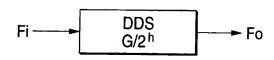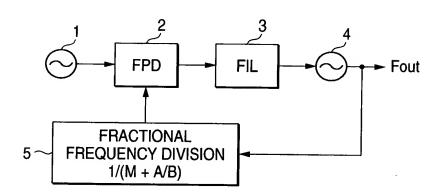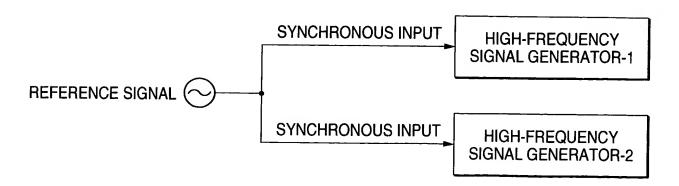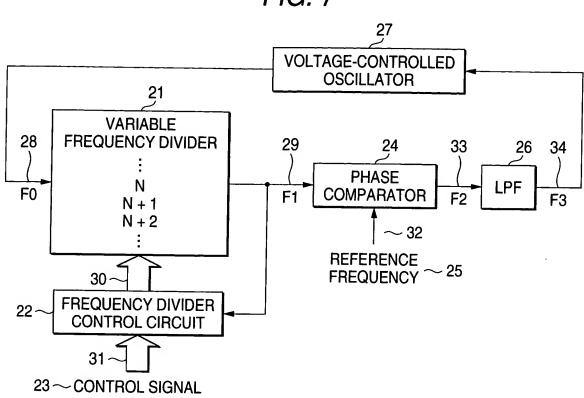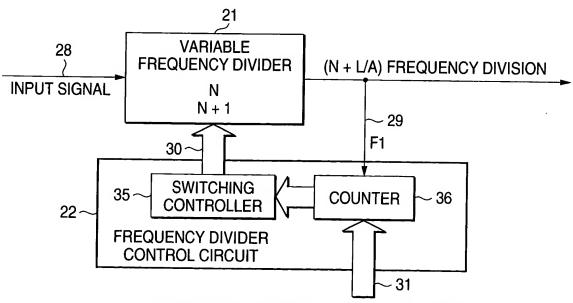4/5

FIG. 7

VOLTAGE-CONTROLLED
OSCILLATOR ~27

21

28
VARIABLE
FREQUENCY DIVIDER
⋮
N
N + 1
N + 2
⋮

F0

29
F1

PHASE
COMPARATOR ~24

33
F2

LPF ~26

34
F3

~32

REFERENCE
FREQUENCY ~25

30

FREQUENCY DIVIDER
CONTROL CIRCUIT ~22

31

23 ~ CONTROL SIGNAL

FIG. 8

28
INPUT SIGNAL

21
VARIABLE
FREQUENCY DIVIDER
N
N + 1

(N + L/A) FREQUENCY DIVISION

29
F1

30

SWITCHING
CONTROLLER ~35

COUNTER ~36

22

FREQUENCY DIVIDER
CONTROL CIRCUIT

31

SWITCHING DECISION VALUE L (FRACTIONAL NUMERATOR)
MAXIMUM COUNT VALUE A (FRACTIONAL DENOMINATOR)

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FIG. 9

REPETITION PERIOD T

FREQUENCY $(N + 1)$
DIVISION
CONTROL (N)

N-FREQUENCY
DIVISION
$(A - L)$ TIMES

$(N + 1)$-FREQUENCY
DIVISION
L TIMES

N-FREQUENCY
DIVISION
$(A - L)$ TIMES

FIG. 10

OUTPUT
SPECTRUM

F_0

FREQUENCY

$F_0 - 1/T$

$F_0 + 1/T$

$2/T$